IN THE CLAIMS

1. (Amended) A memory cell, comprising:

a source region in a horizontal substrate;

a drain region in the horizontal substrate;

a channel region separating the source and the drain regions;

F1

an edge-defined vertical floating gate located above a portion of the channel region and separated from the channel region by a first thickness insulator material;

~~at least one~~ a first edge-defined vertical control gate located above another portion of the channel region and separated therefrom by a second thickness insulator material, wherein the ~~at least one~~ the first vertical control gate is parallel to and opposing the vertical floating gate on a first side of the vertical floating gate, and wherein the ~~at least one~~ the first vertical control gate is separated from the vertical floating gate by an intergate dielectric; ~~and~~

a second edge-defined vertical control gate located on a second side of the vertical floating gate that is parallel and opposing the vertical floating gate and separated from the vertical floating gate by the integrate dielectric; and

an edge-defined horizontal control gate coupled on its opposing sides to top portions of the first and second vertical control gates and separated from the vertical floating gate by the intergrate dielectric.

~~wherein a floating gate capacitance associated with the edge-defined floating gate is smaller than a control gate capacitance associated with the at least one edge-defined vertical control gate, and wherein a greater percentage of a voltage applied to the at least one vertical gate appears between the vertical floating gate and the channel region than between the at least one vertical control gate and the vertical floating gate~~.

2. (Amended) The memory cell of claim 1, wherein ~~the~~ at least one of the ~~vertical~~ control gates has a horizontal width of approximately 100 nanometers (nm).

3. (Original) The memory cell of claim 1, wherein the first thickness insulator material is approximately 60 Angstroms (Å), and wherein the second thickness insulator material is approximately 100 Angstroms (Å).

4. (Original) The memory cell of claim 1, wherein the first thickness insulator material, the second thickness insulator material, and the intergate dielectric include silicon dioxide (SiO2).

F1 Cont.

5. (Original) The memory cell of claim 1, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 Angstroms (Å).

6. (Original) The memory cell of claim 1, wherein the intergate dielectric has a thickness approximately equal to the first thickness insulator material.

7. (Amended) A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

an edge-defined vertical floating gate separated from a first portion of the channel region by a first oxide thickness;

~~at least one~~ a first edge-defined vertical control gate separated from a second portion of the channel region by a second oxide thickness, wherein the ~~at least one~~ first vertical control gate is parallel to and opposing a first side of the vertical floating gate; ~~and~~

a second edge-defined vertical control gate separated from the second portion of the channel region by the second oxide thickness, wherein the second vertical control gate is parallel to and opposing a second side of the vertical floating gate; and

a horizontal edge-defined control gate coupled to top portions of the first and second vertical control gates.

~~wherein a floating gate capacitance associated with the edge defined floating gate is smaller than a control gate capacitance associated with the at least one edge defined vertical~~

~~control gate, and wherein a greater percentage of a voltage applied to the at least one vertical gate appears between the vertical floating gate and the channel region than between the at least one vertical control gate and the vertical floating gate~~.

8. (Original) The transistor of claim 7, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 nanometers (nm).

9. (Original) The transistor of claim 7, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

F1 Cont.

10. (Amended) The transistor of claim 7, wherein the ~~at least one~~ vertical control gates ~~has~~ have horizontal widths of approximately 100 Angstroms (Å).

11. (Amended) The transistor of claim 7, wherein the vertical floating gate separated from a first portion of the channel region includes a first portion of the channel region which is adjacent to the source region, and wherein the ~~at least one~~ vertical controls gate separated from ~~a~~ the second portion of the channel region includes a second portion of the channel region which is adjacent to the drain region.

12. (Amended) The transistor of claim 11, wherein the ~~at least one vertical control gate further includes a horizontal member located above the vertical floating gate, wherein the at least one vertical control gate and the~~ horizontal control gate and the vertical control gates ~~member~~ are separated from the vertical floating gate by an intergate dielectric.

13. (Amended) The transistor of claim 7, wherein a capacitance between the ~~at least one vertical~~ control gates and the floating gate is greater than a capacitance between the floating gate and the channel.

14. (Amended) A floating gate transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first edge-defined vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

a second edge-defined vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness;

a third edge-defined vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness; and

a horizontal gate coupled to top portions of the first vertical gate and the third vertical gate and separated from the second vertical gate by an intergate dielectric, and wherein the first and third vertical gates oppose one another on opposite sides of the second vertical gate and are also separated from the second vertical gate by the intergate dielectric.

F1 Cont.

~~wherein a first capacitance associated with one of the vertical gates is smaller than a second capacitance associated with the remaining vertical gates, and wherein a greater percentage of a voltage applied to the second or third vertical gate appears between the first vertical gate and the channel region than between the second or third vertical control gate and the first vertical gate~~.

15. (Canceled) The floating gate transistor of claim 14, wherein the second and the third vertical gates are parallel to and on opposing sides of the first vertical gate.

16. (Amended) The floating gate transistor of claim 14, wherein the ~~first~~ second vertical gate ~~includes~~ is a floating gate and wherein the second and ~~the~~ third vertical gates and the horizontal gate ~~include~~ are control gates.

17. (Amended) The floating gate transistor of claim 14, wherein ~~first~~ second vertical gate ~~includes~~ is a control gate and wherein the second and ~~the~~ third vertical gates and the horizontal gate are ~~include~~ floating gates.

18. (Canceled) The floating gate transistor of claim 14, wherein the floating gate transistor further includes a horizontal gate member which couples the second and the third vertical gates.

19. (Amended) The floating gate transistor of claim 14, wherein a greater percentage of a voltage applied to the ~~second~~ first and ~~the~~ third vertical gates and the horizontal gate appears between the ~~first~~ second vertical gate and the channel than between the ~~first~~ second vertical gate and the ~~second~~ first and ~~the~~ third vertical gates and the horizontal gate.

F1 Cont.

20. (Original) The floating gate transistor of claim 14, wherein the second and the third portion of the channel region are adjacent the source region and the drain region, respectively.

21. (Original) The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate include polysilicon gates which are separated from one another by silicon dioxide (SiO2).

22. (Original) The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate each have a horizontal width of approximately 100 nanometers (nm).

23. (Original) The floating gate transistor of claim 14, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

24-69. (Previously Canceled)

70. (NEW) A memory cell, comprising:

a horizontal gate coupled to top portions of two opposing vertical gates, and wherein the vertical gates are parallel with one another;

a non-coupled vertical gate separated from the two vertical gates and the horizontal gate by a intergate dielectric, wherein the non-coupled vertical gate separates the two vertical gates.

71. (NEW) The memory cell of claim 70 wherein the horizontal gate and the two vertical gates are control gates and the non-coupled vertical gate is a floating gate.

72. (NEW) The memory cell of claim 70 wherein the horizontal gate and the two vertical gates are floating gates and the non-coupled vertical gate is a control gate.

F1 Cont.

73. (NEW) A memory cell comprising:

a horizontal floating gate coupled to the ends of two opposing and parallel vertical floating gates; and

a vertical control gate that is separated from the floating gates by an intergate dielectric, and wherein the vertical gate is also parallel to and separates the two parallel vertical gates.

74. (NEW) The memory cell of claim 73 wherein the gates are located above a channel region for the memory cell.

75. (NEW) The memory cell of claim 75 wherein the channel region separates source and drain regions of a horizontal substrate for the memory cell.

76. (NEW) A transistor comprising:

a first control gate;

a second control gate;

a third control gate; and

a floating gate;

wherein the control gates surround the floating gate on three sides of the floating gate and are separated from the control gate by an intergate dielectric, and

wherein at least two of the control gates are separated by and parallel to the floating gate.

77. (NEW) The transistor of claim 76 wherein the at least two control gates and the floating gate are vertical gates.

78. (NEW) The transistor of claim 76 wherein the second and third control gates are coupled to the first control gate on their top vertical portions.

79. (NEW) A transistor comprising:

three coupled gates coupled on their ends with one another, where two of the coupled gates are parallel with one another; and

a non-coupled gate surrounded on three sides by the three coupled gates and separating the two parallel gates, and further separated by an intergate dielectric from the three coupled gates.

80. (NEW) The transistor of claim 79 wherein the two parallel gates are coupled indirectly with one another through the remaining coupled gate.

81. (NEW) The transistor of claim 79 wherein the three coupled gates are control gates and the non-coupled gate is a floating gate.

82. (NEW) The transistor of claim 79 wherein the three coupled gates are floating gates and the non-coupled gate is a control gate.